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Laser Processing of Silicon on Sapphire (SOS) for Fabrication of Bipolar Transistors

B. W. Offord
S. D. Russell
NOSC

K. H. Weiner
Lawrence Livermore National Laboratory

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NAVAL OCEAN SYSTEMS CENTER
San Diego, California 92152-5000

J. D. FONTANA, CAPT, USN
Commander

R. M. HILLYER
Technical Director

ADMINISTRATIVE INFORMATION

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Released by
G. A. Garcia, Head
Research and Technology
Branch

Under authority of
H. E. Rast, Head
Solid State Electronics
Division

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INTRODUCTION

The very large scale integration (VLSI) of microelectronic devices and the future downscaling of electronic systems require dielectric isolation to overcome problems associated with conventional junction isolation such as latch-up, unscalable vertical dimensions, and increased leakage at elevated temperatures (Ref. 1). Silicon-on-insulator (SOI) technologies achieve this dielectric isolation. SOI technologies promise to offer increased device performance by reducing parasitic capacitance and interconnect delay and by increasing radiation hardness. Many examples of SOI technologies are known, but they have had limited degrees of success and have lacked process maturity (Ref. 2). In SOI technology, small islands of silicon which contain the individual device are fabricated on an insulating substrate and are then interconnected in the normal way. Problems associated with these technologies generally are due to the difficulty of achieving or the inability to achieve "device quality" silicon on an insulating layer. "Device quality" requires silicon layers having neither crystallographic defects nor impurities which prevent the fabrication of functioning devices.

One SOI technology that has been investigated employs epitaxially grown silicon-on-sapphire (SOS). Early attempts at fabricating device quality SOS have been documented (Ref. 3). Since then, techniques have been developed to improve the near interfacial region for thin silicon layers on sapphire such as solid-phase epitaxy (SPE), double-solid-phase epitaxy (DSPE), and solid-phase epitaxy and regrowth (SPEAR) (Ref. 4–6). These techniques, however, do not provide device quality material for devices having more stringent materials requirements, such as bipolar junction transistors and charge-coupled devices (CCDs), which require thicker films and high-quality epitaxial layers (Ref. 7). Previous attempts at fabricating bipolar devices in SOS have been blocked by materials defects (Ref. 8) (see Fig. 1). The inability to achieve silicon epitaxially grown on sapphire without dislocations, slip planes, and twin defects results in a failure mechanism for devices caused by "diffusion pipes." Diffusion pipes are crystallographic defects which allow paths for dopant atoms to diffuse (or migrate) during high-temperature anneals. The anneals are critical in the processing of semiconductor devices in that they allow the electrical activation of ion-implanted dopant atoms. Therefore, the diffusion of dopant from one junction into another (e.g., from the emitter to the base) results in leaky or shorted devices. It is not surprising, then, that the research and development of high-quality crystalline films on sapphire and of novel processing techniques are important to improved SOS device fabrication.

The laser processing of materials has been investigated for a variety of applications and is being used in the semiconductor processing of silicon VLSI in such applications as laser-assisted etching (Ref. 9, 10), chemical vapor deposition (CVD) (Ref. 11), and alloy formation (Ref. 12), to name a few. The laser activation of ion-implanted dopant has long been known as an alternative to conventional furnace annealing (Ref. 13, 14), and techniques such as gas immersion laser doping (GILD) have proven valuable in the formation of shallow junctions in bulk silicon (Ref. 15, 16). In addition, the excimer laser annealing of implant damage in bulk silicon has been demonstrated (Ref. 17). These studies, however, have been limited to examining the processing of high-quality bulk silicon and have not explored the unique requirements of SOS.

Excimer laser processing has shown advantages over standard processing in the fabrication of bipolar transistors in bulk silicon (Ref. 18). The independent control of emitter and base junction depths, abrupt junctions, square doping profiles, and a high degree of repeatability are some of these advantages. The Naval Ocean Systems Center (NOSC) and the Lawrence Livermore National Laboratory (LLNL) proposed that these advantages could be used with SOS to make high-speed, dielectrically isolated bipolar transistors. Laser processing, with its extremely low thermal cycles, could reduce or eliminate emitter-to-collector shorts due to the diffusion of dopant through the emitter-base junction.

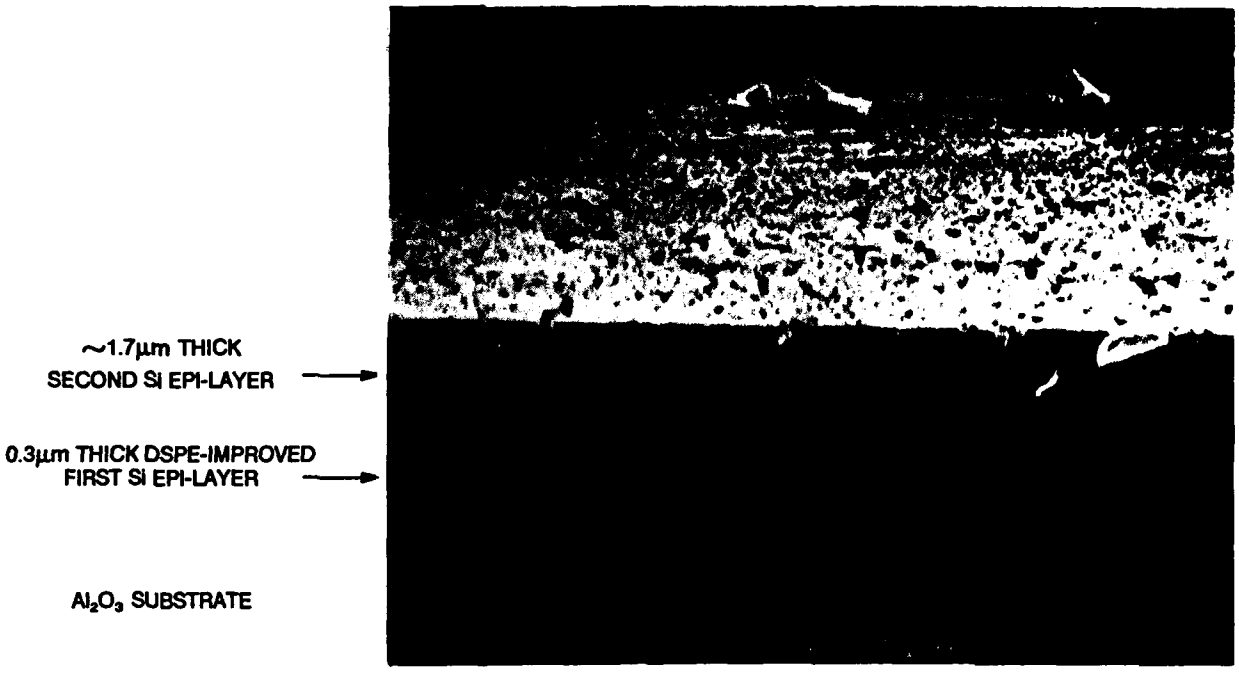


Figure 1. 2.0μm SOS starting material, cleaved and defect etched.

Another possible advantage of laser processing on SOS is the recrystallization of the active regions of transistors, thereby reducing defects by terminating them on a melt front.

Incorporating excimer laser processing into a VLSI environment is of critical importance to the ultimate usefulness of advanced devices. The excimer laser processing steps demonstrated at LLNL and the bipolar-on-SOS processes demonstrated at NOSC were merged into a single process compatible with standard processing techniques and designed to lead toward a high-performance, high-yield, reproducible and reliable fabrication sequence. This effort was to address the requirements of both laser processing and state-of-the-art VLSI processing—requirements needed to develop a smoothly integrated, complete process. After the processing integration questions were addressed, a single full-process run was completed in which both bulk and SOS substrates were used.

SOS wafers (100-mm diameter) used in this effort were 2.0-μm-thick *n*-type silicon epilayer on a DSPE-improved *n+* type silicon epilayer on sapphire supplied by the Stanford Research Institute (SRI). These wafers represented the best available SOS material for bipolar applications. NPN bipolar transistors were fabricated in this material by using combinations of furnace and laser annealing and variations in processing. LLNL provided the laser processing, while NOSC's Battery Ashburn North microelectronics lab performed the remaining processing, device modeling, materials characterization, and electrical testing.

This collaborative effort between LLNL and NOSC is described in this report. A discussion of laser processing techniques and requirements will be followed by a description of the fabrication of transistors in SOS. Next, the results of the electrical tests of the transistors are presented. Finally, the conclusions derived from these tests are summarized.

PROCESS DEVELOPMENT

Using parameters developed under NOSC's bipolar effort, a process was designed with slightly modified parameters to accommodate the different steps needed to laser-anneal the base, emitter, and extrinsic base implants (see Fig. 2). There were two major processing lots in FY90: lots 787 and 819. Lot 787 was processed by laser-annealing the base and implanting the emitter and extrinsic base. At this point, it was noticed that the emitter, collector, and extrinsic base regions were covered with a film subsequently attributed to polymer formation in the plasma etching of the contacts. A number of methods were used to remove this polymer, but none were successful, and the lot was not processed further. What was gained from this lot was (1) knowledge of the process to dielectrically isolate transistors by using a patterned KOH etch, (2) knowledge of how to laser-anneal the base implant by using 100% aluminum on SiO_2 as a mask on SOS and bulk, and (3) knowledge that a different process needed to be developed to self-align the contact etch and an aluminum laser mask. Details of these results and related process developments are described below.

MODELING

Implants were modeled using SUPREMIII, and the energies and doses were chosen to obtain the doping profiles in Fig. 3. The input parameters for the computer modeling were as follows:

1. The laser-annealed base redistributes dopant uniformly to a depth of 300 nm.
2. The remaining dose in the base after implanting through 60 nm of oxide is 9.5E12 cm^{-2}.
3. The background doping is 1E16 cm^{-3} for SOS.
4. The laser-redistributed emitter/collector and extrinsic base implants have a depth of 0.15 μm–0.25 μm, depending upon the melt duration.

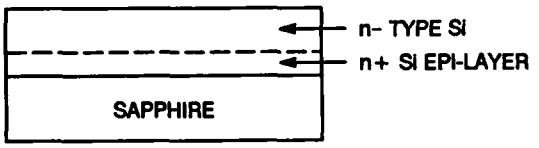
With these parameters, the base width should vary from 150 nm to 50 nm, and the base dose should vary from 4.5E12 cm^{-2} to 1.5E11 cm^{-2}. The base doping concentration was 3E17 cm^{-3}.

KOH ETCH

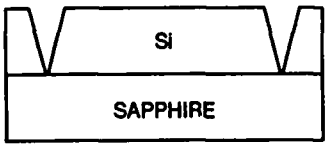
Bipolar transistors need to be isolated from each other to prevent parasitic leakage and parasitic transistor action. To optimize performance, they also need a buried, highly doped collector to reduce series resistance. In bulk silicon, this is usually accomplished by a masked implant and subsequent epitaxial growth. Isolation is usually achieved by using guard rings of dopant to junction-isolate the active regions. On SOS, however, the technique implemented here is much simpler and more effective. The transistors are isolated by etching the silicon to the sapphire substrate, leaving islands of silicon where transistors will be formed. The buried layer is formed by implantation into 3000 Å of SOS over the entire wafer and then a silicon epitaxial layer is grown to a thickness of 2.0 μm.

To etch the silicon, we used a KOH solution to selectively etch the <100> plane, leaving a slope to the sidewalls of 54.7 degrees. This leads to two advantages: (1) sloped sidewalls mean better step coverage for the metal layer (without using any planarization techniques), and (2) an automatic collector plug is obtained with the emitter/collector implant, thereby further reducing the collector series resistance. The recipe that we used is as follows:

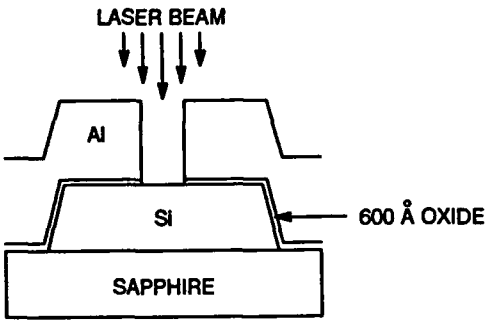
KOH (45%soln)	741 ml
H_2O	1400 ml
1-propanol	500 ml



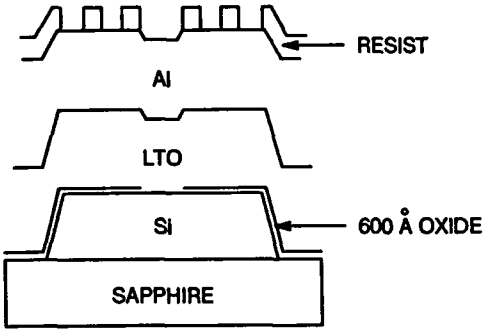
(a) Starting material.



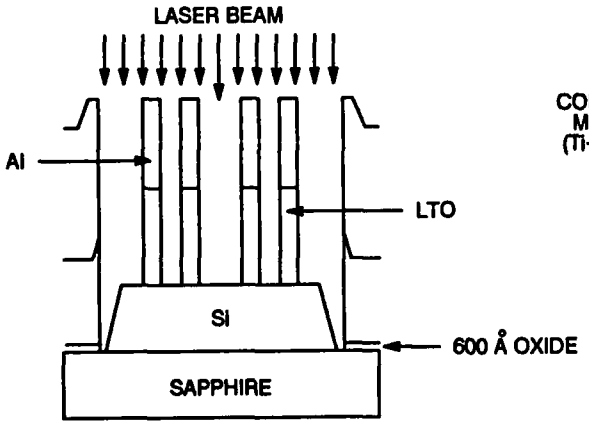
(b) After patterned KOH etch.



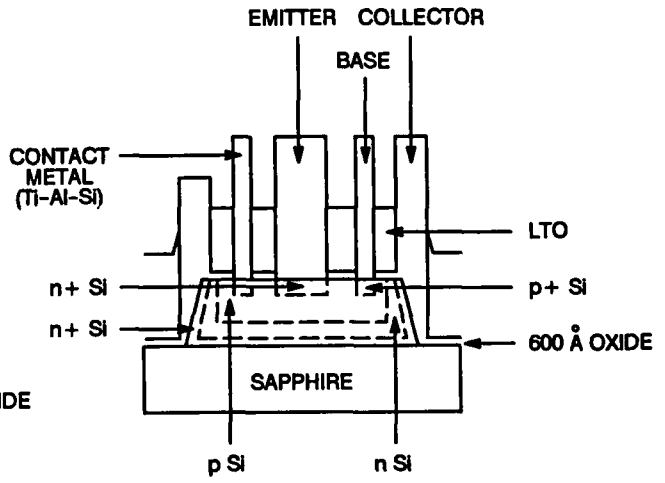
(c) Laser anneal of base implant.



(d) Photo step for contacts.



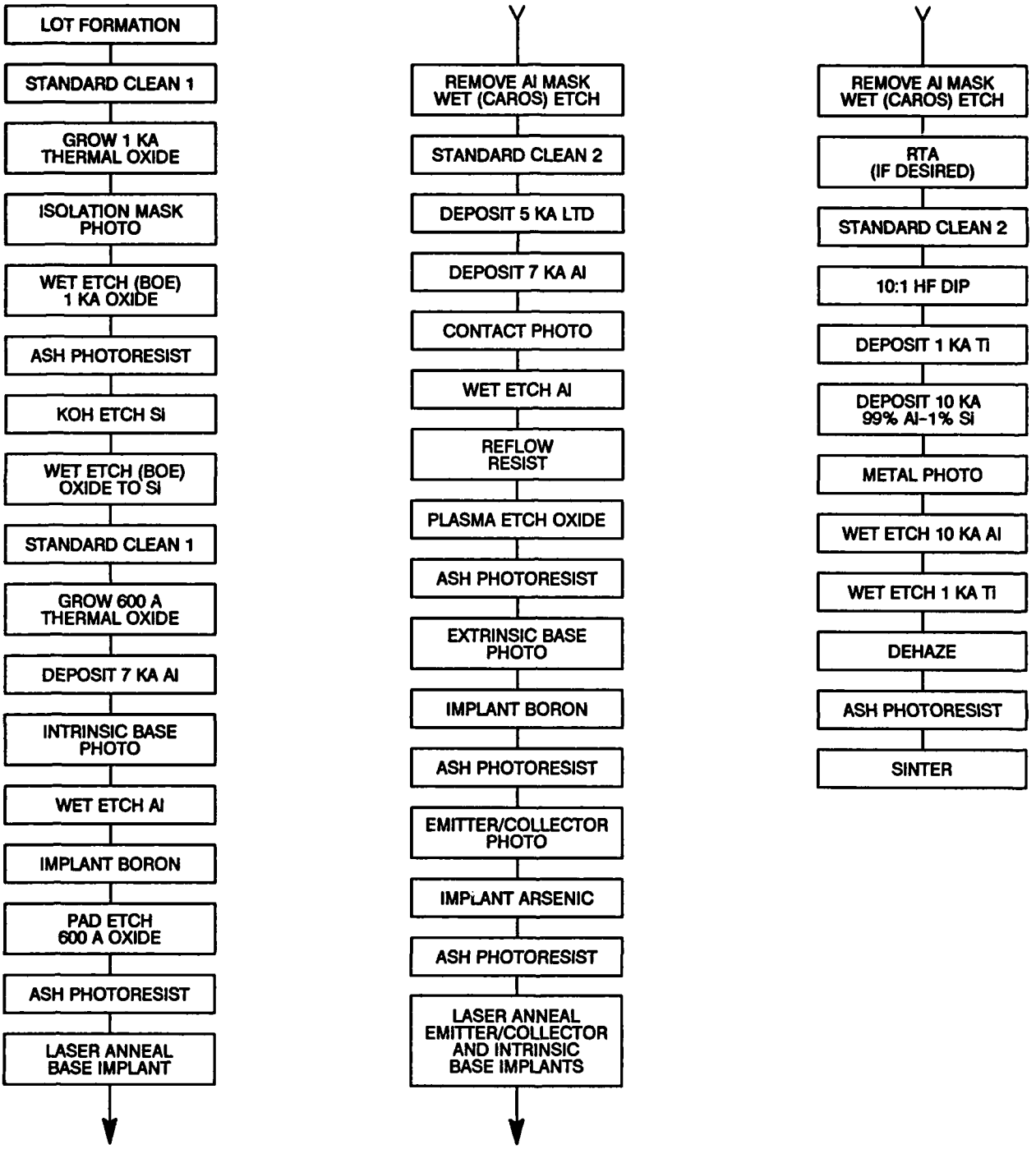
(e) Laser anneal of emitter, collector, and extrinsic base implants.



(f) Final structure.

(Contd)

Figure 2. Process for laser-annealing base, emitter, and extrinsic base implants.



(g) Detailed process flow.

Figure 2. Continued.

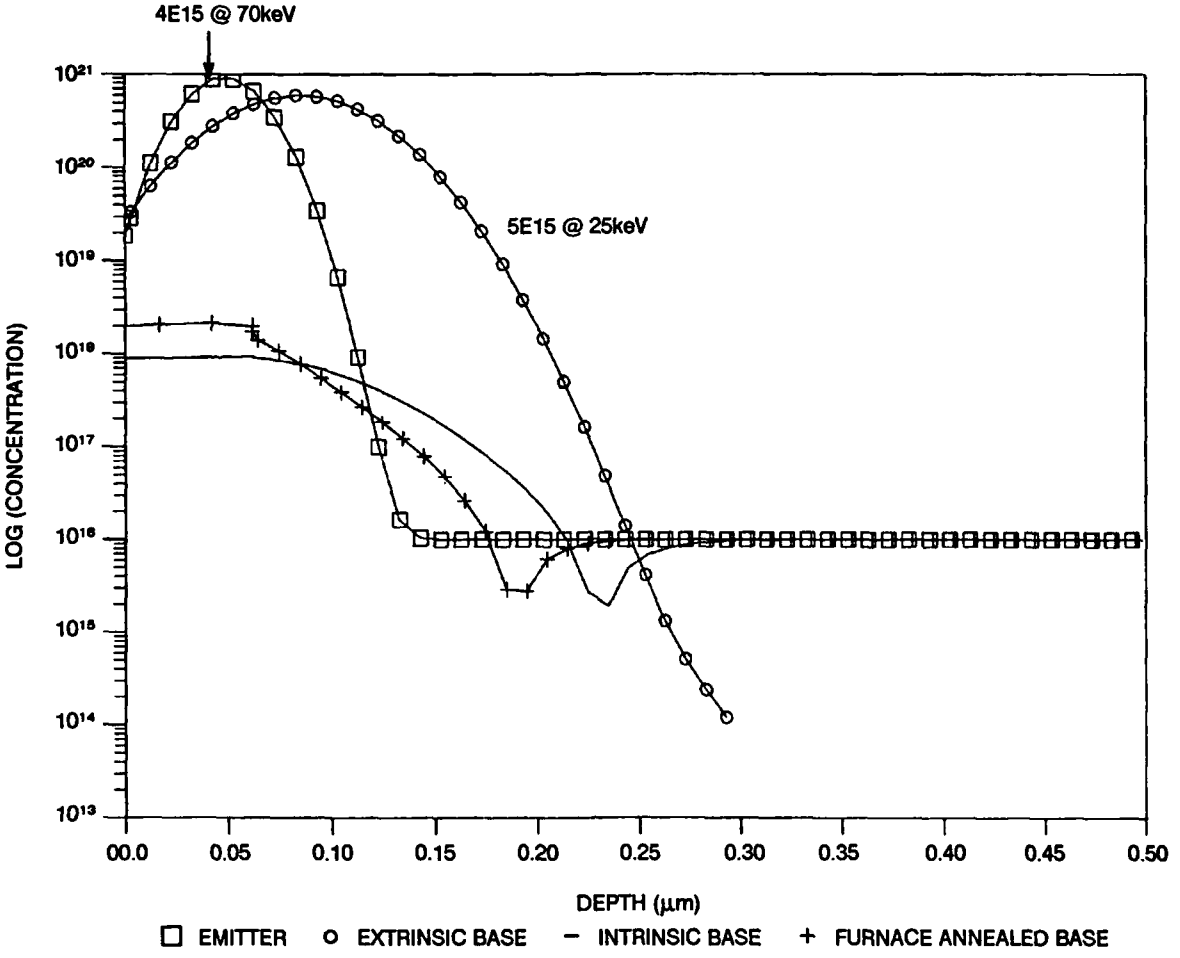


Figure 3. Lot 819 simulated doping profiles.

The etch was stirred with a magnetic stirrer and the temperature was kept at 80°C. Agitation and temperature control are very important to this etch. Insufficient agitation and temperatures below 80°C will result in a very low etch rate. The etch is endpointed on the SOS wafers visually by observing the wafer become transparent in the field regions. Since the selectivity of this etch to crystallographic planes other than the <100> is 100:1, an overetch is not harmful. Figures 4 and 5 are SEM microphotographs of the resulting structure on bulk and SOS, respectively. Note that the corners on the SOS sample behave the same as on bulk-etching along the <311> plane, as theory predicts. Although this produces some rounding of the corners, it is acceptable for our application.

Figure 4. SEM photo of bulk KOH etch.

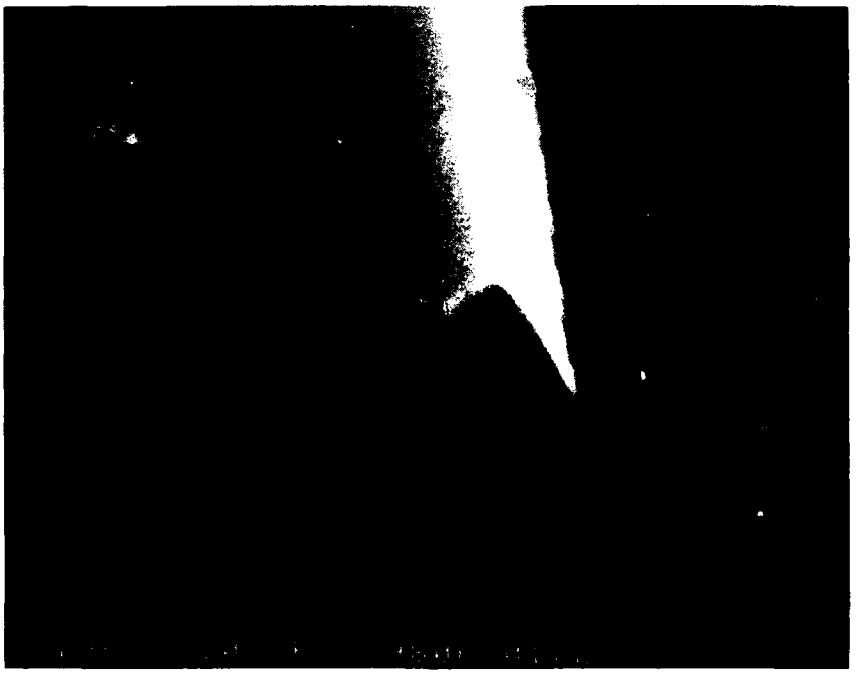


Figure 5. SEM photo of SOS KOH etch.

LASER MASK REQUIREMENTS

The masked laser step to anneal the base and emitter/collector implants is the heart of the laser bipolar process. The ideal masking structure for the laser anneals is shown in Fig. 6. The material used to mask the laser must be a high-quality reflective material at UV wavelengths that is resistant to ablation. Previous research at LLNL and Image Micro Systems has disclosed the satisfactory use of 100% pure aluminum because it meets these criteria. Experiments were performed at NOSC on the reflectivity of sputtered aluminum (Al) layers to be used as a mask for laser processing. The Al test layers were 100% Al with and without a 350°C preheating. No damage was detected on these layers when subjected to 20 pulses of ultraviolet irradiation at 248 nm with fluences above 1 J/cm^2 (which is sufficient to melt silicon). A secondary ion mass spectroscopy (SIMS) analysis showed no Al driven into the silicon at the edge of the Al mask, thereby allowing the use of our metalization as a laser mask. NOSC's Varian load-locked system was used and found to be superior in reflectivity to non-load-locked systems. This provided an increased flexibility in laser processing by allowing the use of increased laser fluence and its corresponding increase in melt duration and junction depth without ablation of the aluminum mask.

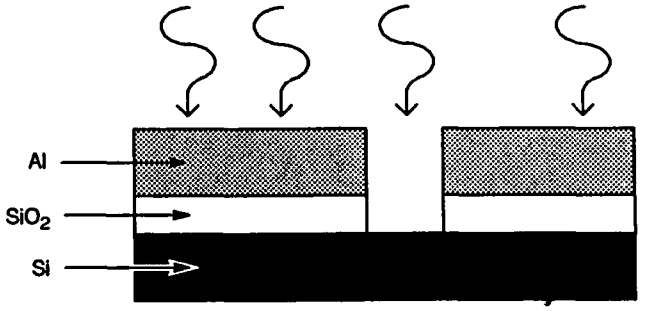


Figure 6. Idealized masking structure for laser annealing.

ALUMINUM-TO-OXIDE SELF-ALIGNMENT

To address the problem of etching contacts that are self-aligned to the aluminum laser mask, lots 818 and 836 were started. Our bipolar process requires that contact holes in SiO_2 be cut before our emitter/collector implants, and this puts more constraints on our masking techniques than a conventional process in which implants are performed and contacts are aligned to these implants. There are a variety of ways to attempt to achieve the structure shown in Fig. 6. The various methods tried are shown in Table 1. Trials 1–4 were methods that had photoresist (PR) present during the etches of aluminum and silicon dioxide. Trial 5 had the PR ashed off after an aluminum wet etch and then the oxide was plasma etched. Trial 6 had the PR reflowed after a wet metal etch to pull back the resist to the aluminum edge. Trials 1 and 2 resulted in structures that were unacceptable for the requirements of laser processing because of undercutting of the layers by the wet etches.

Table 1. Methods used to obtain an idealized masking structure.

	Al		SiO_2	
Trial*	Wet	Dry	Wet	Dry
1	X		X	
2	X			X
3		X		X
4		X		X
5	X			X
6	X			X

* In trials 1–3, photoresist was present throughout.
In trial 4, Al was dry etched, 2000 Å of oxide was wet etched, and 3000 Å was dry etched.
In trial 5, photoresist was ashed off after the Al wet etch.
In trial 6, photoresist was reflowed after the Al wet etch.

Special attention was paid to trial 3 (dry/dry) since it was the most desirable profile and ostensibly the most reproducible of all the profiles. SEM photomicrographics of trial 3 profile show vertical sidewalls of Al and SiO_2 very much self-aligned to each other (Fig. 7 and 8). The photos also show, however, a particulate problem that shows up after the Al is dry etched and that subsequently micromasks the dry oxide etch. This is unacceptable for subsequent implantation and the laser annealing of the surface. This particulate problem was initially attributed to the Al deposition, but subsequent observation of a deposited 100% Al film and an Al/1%Si film under dark-field illumination showed no particulates.

Observation of previous lots shows that wet etching the Al removes any evidence of speckling and leaves no particulates. Dry etching of the bare 100% Al wafer also removed any evidence of speckle and particles. This leads us to believe that PR is a contributing factor to the particulate problem and not the speckling of the Al. However, one reference (Ref. 19) suggests that the particulates are caused by hillocks or surface roughness in the deposited Al film. The reference suggests a dip in dilute HF to remove the particulates. This was tried to an extreme in trial 4 where 2000 Å of oxide was removed before the rest of the oxide was dry etched. However, since particulates remained, this was only partially successful.

Trial 5 was an attempt to use the aluminum as a mask for a plasma etch of the oxide. Both the Tegal 703 and the Tegal 1513 plasma oxide etchers at NOSC were used with a $CHF_3/SF_6/He$ chemistry. This chemistry resulted in polymer formation in the contact holes. A CHF_3/O_2 chemistry might be used to alleviate this problem. However, as evidenced by the other trials, if there is PR present, the $CHF_3/SF_6/He$ chemistry can be used successfully.

Trial 6 involved reflowing the resist after a wet metal etch. This reflow consists of an oven bake at 175°C for 30 minutes (wafers are to be put into the furnace while it is hot) and results in the PR pulling back to the Al edge due to surface tension. The oxide can then be dry-etched with PR present and be self-aligned to the aluminum mask. The SEM of the resultant structure is shown in Fig. 9 and 10.

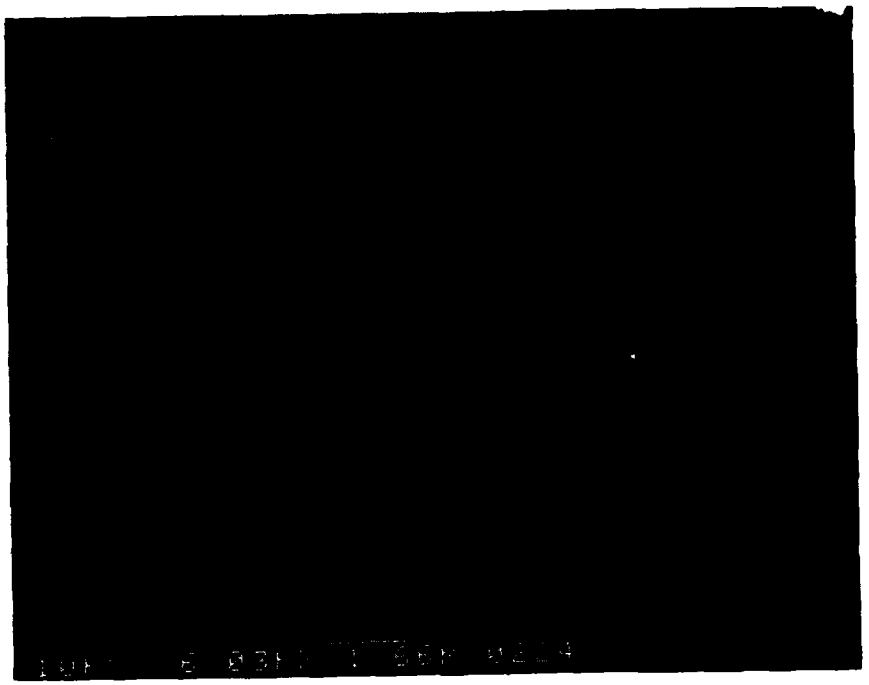


Figure 7. SEM photo of DRYTEK-etched Al.

Figure 8. SEM photo of DRYTEK-etched Al, TEGAL etched oxide.

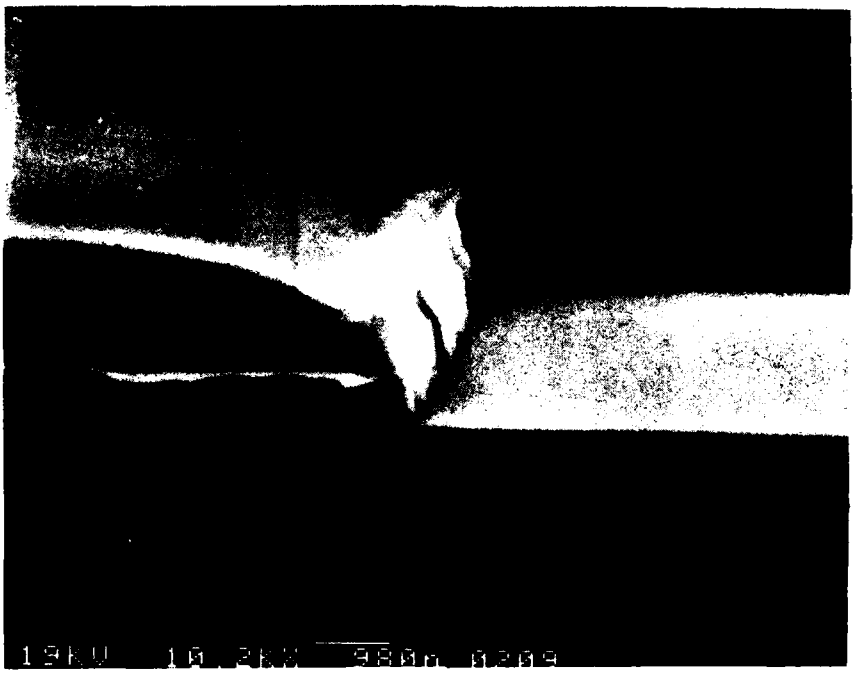


Figure 9. SEM photo of reflowed resist, oblique view.

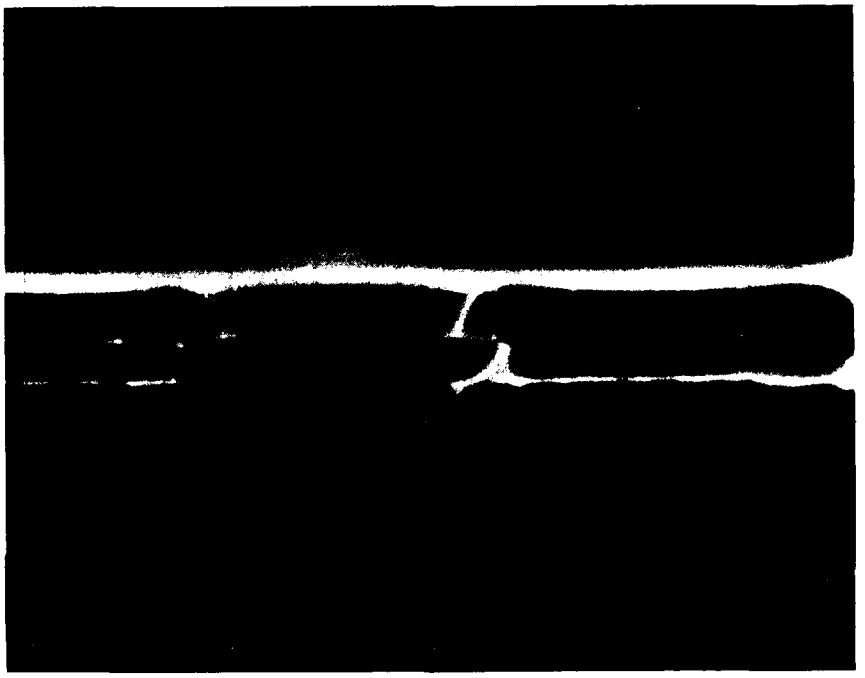


Figure 10. SEM photo of reflowed resist, cross-sectional view.

FABRICATION OF BIPOLAR TRANSISTORS IN SOS

After these results were obtained, the second full process run was started (lot 819). This was to incorporate the etching process developed in lots 818 and 836. Lot 850 was also started to obtain spreading resistance (SR) and SIMS profiles on unpatterned SOS wafers of the laser-annealed intrinsic and extrinsic bases. Lot 819 took 15 weeks to process, which includes 3 weeks of sending wafers to and from LLNL for laser processing. A SEM photomicrograph of a finished transistor is shown in Fig. 11. The transistor is island-isolated and has an emitter dimension of 1x8 μm.

Groups of wafers in lot 819 were processed differently to obtain comparisons of the furnace and laser annealing of the base implant. In addition, each wafer was processed with variations in the emitter depths, thereby giving a comparison of different base widths. Table 2 summarizes these wafer variations.

Table 2. Wafer processing conditions.

	Wafer Number				
Processing Techniques	1, 2	3	D73, D74, 4	D70, D71	D72
Furnace Base	X	X		X	
Laser Base			X		X
Stanford Oxide Etched		X	X		
NOSC Oxide Etched	X			X	X

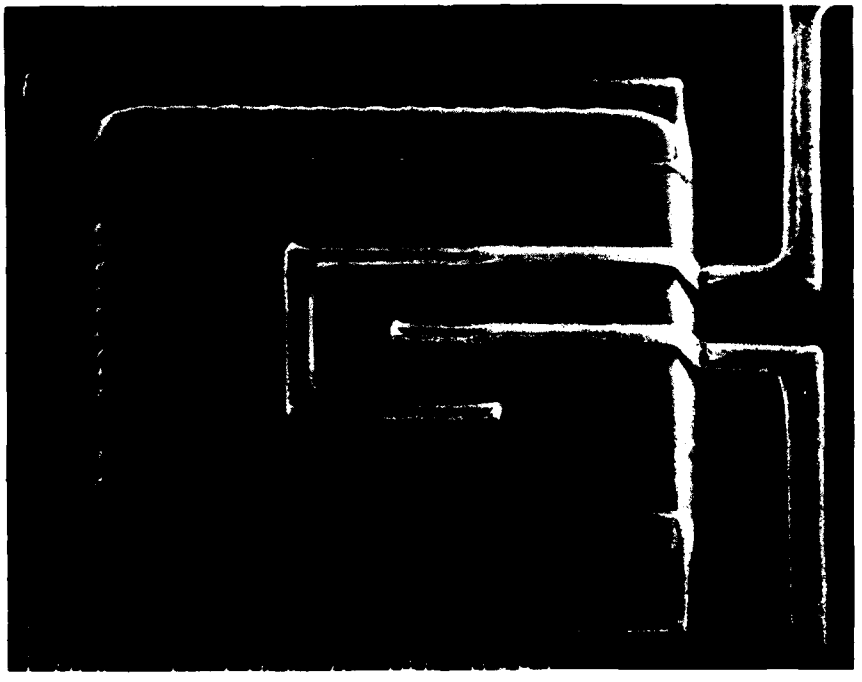


Figure 11. SEM photo of finished NPN transistor.

RESULTS

DOPANT PROFILES

The resulting dopant profiles as measured by SIMS and SR are shown in Fig. 12–16. The most important feature to note in these figures is the very abrupt junctions in the laser-annealed dopant profiles. Recent theoretical models of desired doping profiles for high-speed bipolar transistors have shown that uniform distribution of the base dopant can increase the base transit time, thereby enhancing device performance (Ref. 20). Conventional annealing techniques cannot achieve these profiles because of the solid state diffusivity of the dopant atoms in silicon and the required subsequent high-temperature processing steps. The uniform profiles shown in Fig. 12–16 exhibit abrupt junctions, thereby allowing ultra-narrow base widths. Furthermore, laser activation of the emitter region, unlike conventional diffusion techniques, does not detrimentally affect the dopant profile of the base.

BASE-COLLECTOR DIODE DATA

Base-collector diodes were tested and ideality, leakage currents, and breakdown voltages were measured. Ideality factors were derived from the forward-biased characteristics in two places, at the diffusion-dominated region and, at low voltages, the recombination-dominated region. The ideality factor, η, is a relative measure of the quality of the junctions in the transistor when forward biased. An η of 1.0 indicates that diffusion currents are dominating the diode characteristics, while an η of 2.0 indicates that recombination-generation is the dominant current mechanism. Because of the doping of the base and collector, the depletion region extends mostly into the collector and the ideality factor reflects the collector region more than inside the base region. The large ideality factors in the SOS devices indicate recombination from such sources as heavy metals or crystallographic defects. Junction leakage currents are also a measure of junction quality and were evaluated at a reverse bias of −5.0 V. Breakdown voltages were measured on transistors, except in the case of the SOS wafers, where the base-collector breakdowns were measured off of separate base-collector diodes (no emitter present) because of excessive emitter-collector leakage. These results with typical values are summarized in Tables 3 and 4. Leakage currents on the bulk wafers were typically 7E−08 A/cm^2 and for the SOS wafers were 2E−06 A/cm^2. These numbers were comparable to other work done with furnace annealing in bulk and SOS wafers processed at NOSC.

Table 3. Measured diode parameters.

Parameter	Furnace Base		Laser Base	
	Bulk (3)	SOS (D70)	Bulk (4)	SOS (D74)
Leakage (A/cm^2)	7.0E−08	2.0E−06	2.0E−07	1.0E−05
Ideality*	1.0–1.1	1.15–1.5	1.0–1.15	1.25–1.55

* First number is ideality in the diffusion-dominated region of the current; second is taken from the recombination-dominated region.

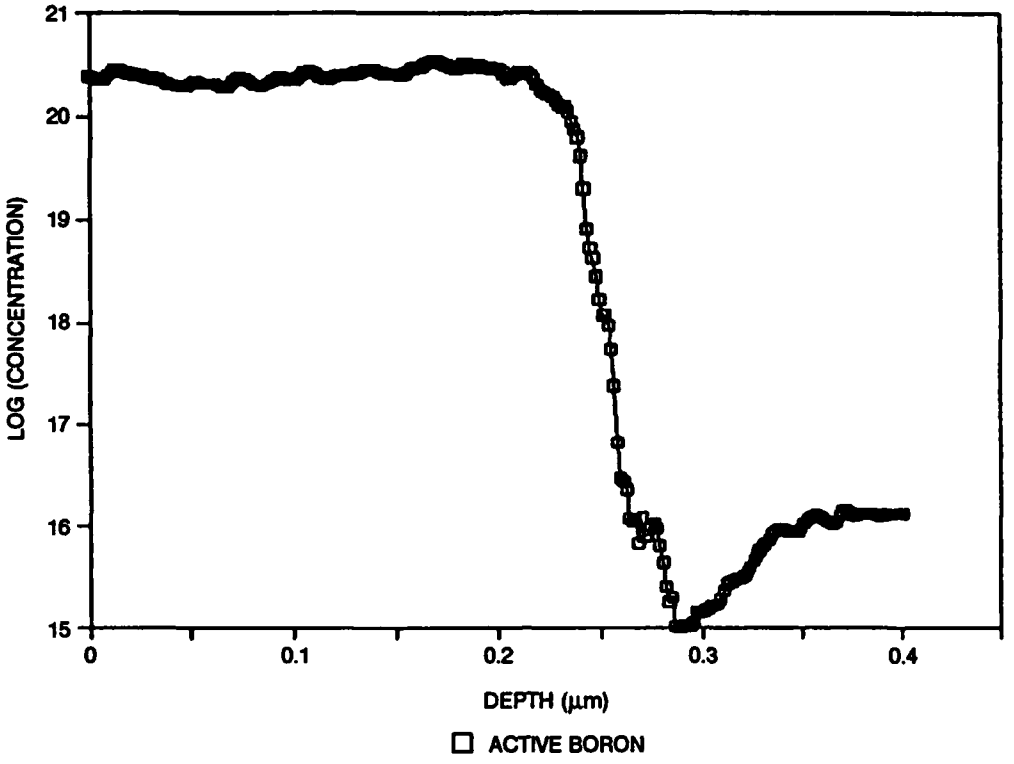


Figure 12. Doping profile of laser-annealed (100 ns) extrinsic base.

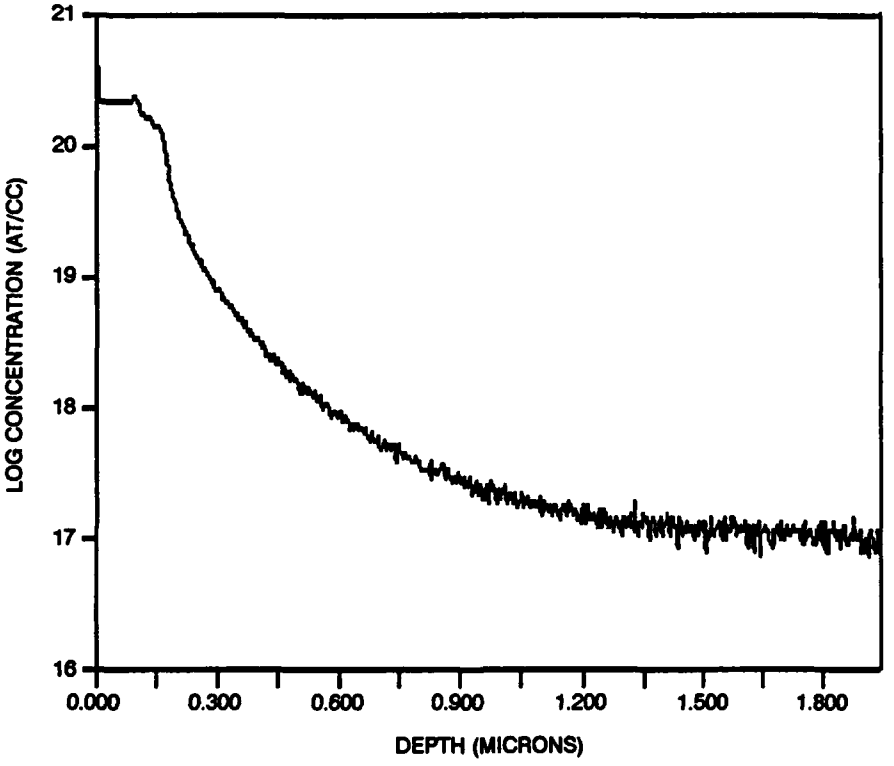


Figure 13. SIMS profile of laser emitter.

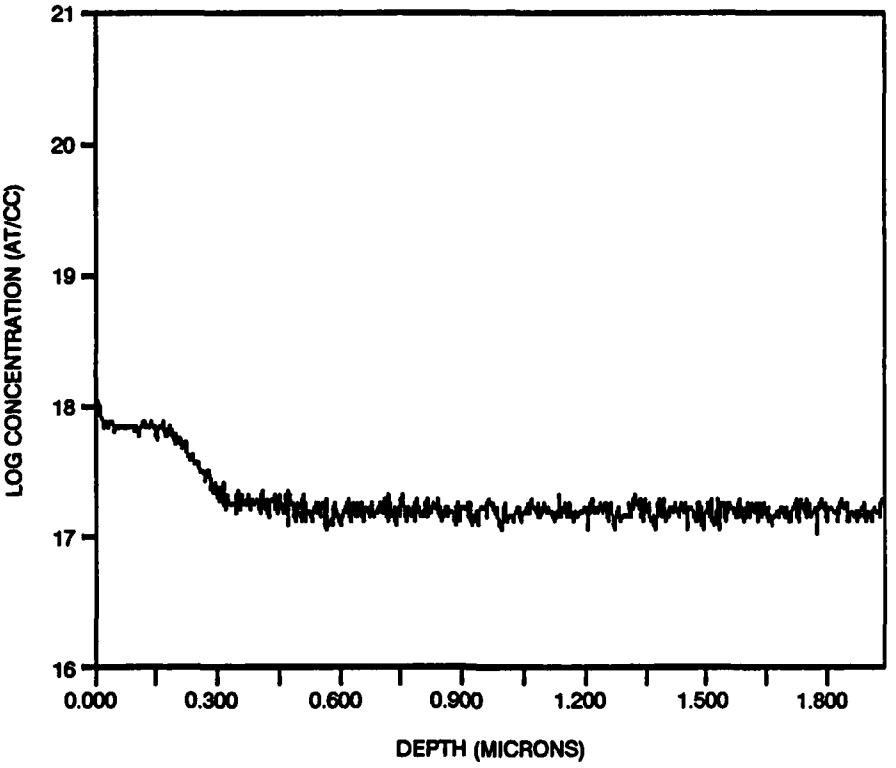


Figure 14. SIMS profile of laser base.

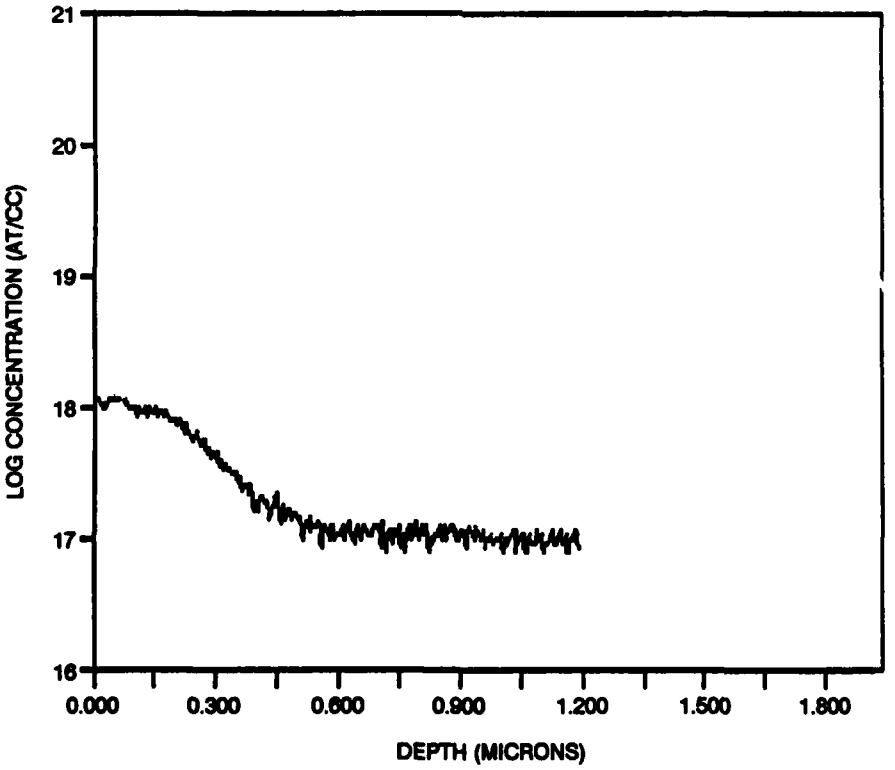


Figure 15. SIMS profile of furnace base.

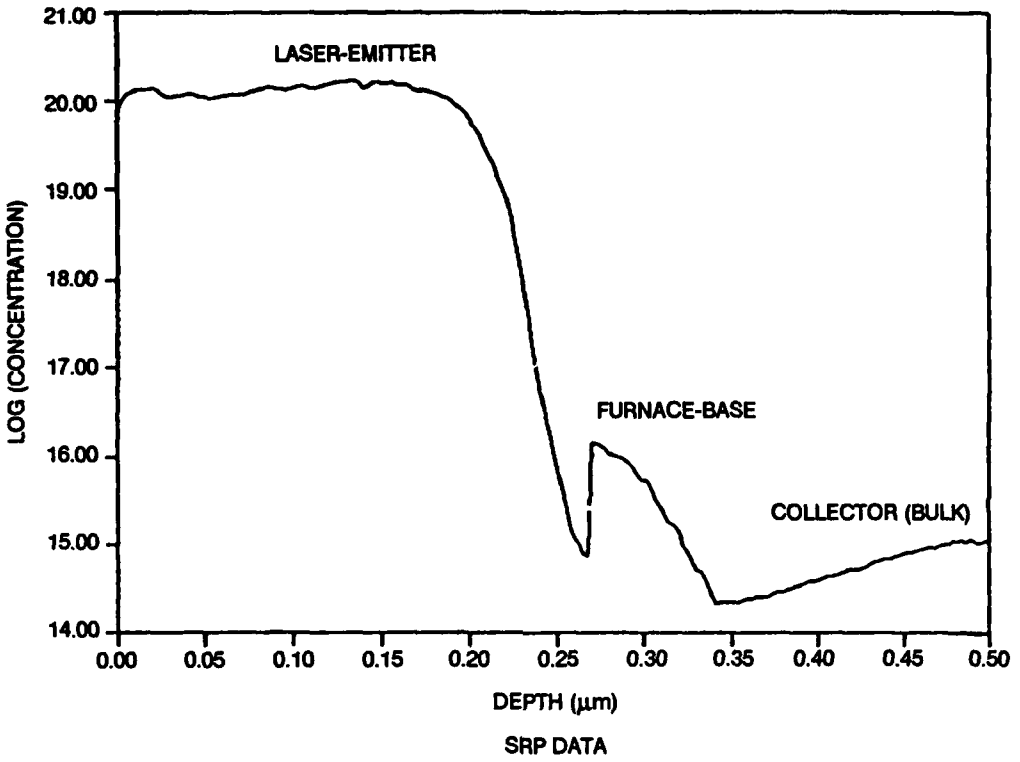


Figure 16. Spreading resistance profile of emitter/base on bulk test wafer.

Table 4. Diode breakdown voltages.

	Wafer Number				
Junction	1, 2	3	D73, D74, 4	D70, D71	D72
Base-Emitter (V)	-6.0	-6.0	-6 (soft)	-6 (soft)	-6 (soft)
Base-Collector (V)	-55	-40	-25*	-26*	-20*

* Data on breakdown taken off separate BC diodes.

NPN TRANSISTOR DATA

Devices were fabricated by using three different laser fluences for the emitter anneal. These different fluences correpond to a variation in melt duration and metallurgical junction depth. The degree of diffusion along crystallographic defects is determined by measuring the collector current (I_c) versus the forward voltage (V_{BE}). Figure 17 shows these data for an NPN transistor with a 1 x 8-μm emitter geometry for various melt durations. Devices with melt durations of 83 ns exhibit significant leakage, with collector current ideality factors exceeding ~1.2. Decreasing the melt duration to 68 ns, by decreasing the laser fluence, results in an improvement in ideality. Melt durations of 57 ns exhibited the most ideal I-V characteristics, with ideality factors ~1.05. These results suggest that unwanted diffusion of dopant in SOS material with crystallographic defects can be inhibited by the nanosecond

thermal processing employed with the excimer laser. These preliminary results have been presented at the 1990 IEEE SOS/SOI Technology Conference (Ref. 21).

Transistors were measured across each wafer, and gummel plots were obtained for the base collector voltage (V_{BC} = 0.0 V) with melt durations for the emitter of 57, 68, and 83 ns (Fig. 18–21). A comparison between the different melt depths in both wafer 3 and wafer D70 reveals an interesting trend. The base currents become more ideal with deeper melt depths (while the collector current on wafer D70 has more leakage with deeper melt depths). This phenomenon can be attributed to unannealed damage from the extrinsic base implant. Only the deepest melt will anneal out all the damage caused by the high-dose extrinsic base implant (see Fig. 3). This will also have a dramatic effect on ideality, as seen in Table 3. Research at LLNL on bulk silicon discovered after this lot was finished that a rapid thermal annealing after laser processing may alleviate this problem by annealing out any residual damage caused by implantation. However, undesirable diffusion of dopant along the aforementioned diffusion pipes may prove this technique inappropriate for SOS. A shallower extrinsic base implant may also help solve this problem.

Details of this diffusion effect are observed on all the wafers. The collector current on wafer D70 shows higher leakage with increased melt depth. This suggests that the longer times and resulting shorter base widths allow dopant to diffuse along crystal dislocations through the emitter-base-collector junctions. Wafer D74 (laser base) also shows this behavior of higher collector leakage with deeper melt depths, but on only one SOS device with a laser-annealed base have we seen base current that was not extremely leaky (this occurred on a device with the longest melt time, reinforcing the idea of longer melt times annealing out damage). Beta vs. IC curves are plotted on a log-log scale for both SOS and bulk wafers and are shown in Fig. 22 and 23, respectively. These curves show the effect of longer laser melt durations on the base width, resulting in higher betas. The SOS curves reflect the excessive leakage currents and nonideality of the base that are apparent in the gummel plots, while the bulk curves are not leaky but are also not flat over a range of collector currents, indicating excessive recombination currents. These curves show that betas near 100 were achieved in SOS over a limited operating range. The range is limited because of leakage current at lower voltages, which we attribute to diffusion pipes and recombination current.

The difference between the electrical characteristics of the laser- and furnace-annealed bases can be attributed to one of two differences in processing: (1) the laser base can have remaining implant damage at the edges of the mask from the laser annealing almost entirely vertically, thereby not annealing the boron that straggled laterally from the implant, and (2) because of the requirements for the laser activation of the base, the surface of the laser base is covered with a deposited, not thermally grown oxide as is the furnace base. Deposited oxides can cause uncontrolled surfaces, thereby creating surface recombination and even inversion at the surface, either one of which can be the cause of excessive leakage currents.

A family of curves for typical devices with 83-ns emitters is shown in Fig. 24 and 25. These figures show functional behavior of the transistors both on bulk and SOS, with the narrowest base fabricated in the lot. The SOS device shows punchthrough behavior, which the bulk device does not. We attribute this to the differences in collector doping and hence a difference in base width between the bulk and SOS. The bulk wafers had a collector concentration of 1E15 cm^{-3} compared with 1E16 cm^{-3} for the SOS. This will have the effect of reducing the base width for the SOS devices compared to the bulk devices. A family of curves for the 57-ns annealed emitters is shown in Fig. 26 and 27 (bulk and SOS, respectively) and does not show this punchthrough behavior.

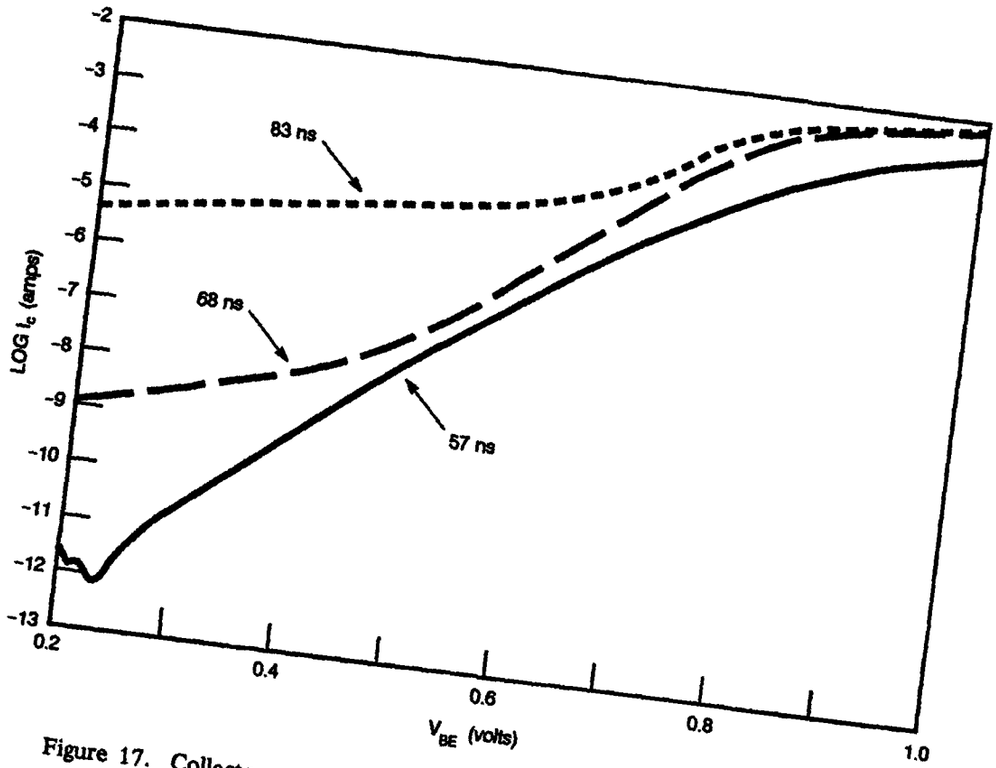


Figure 17. Collector current of an SOS NPN transister vs. melt duration.

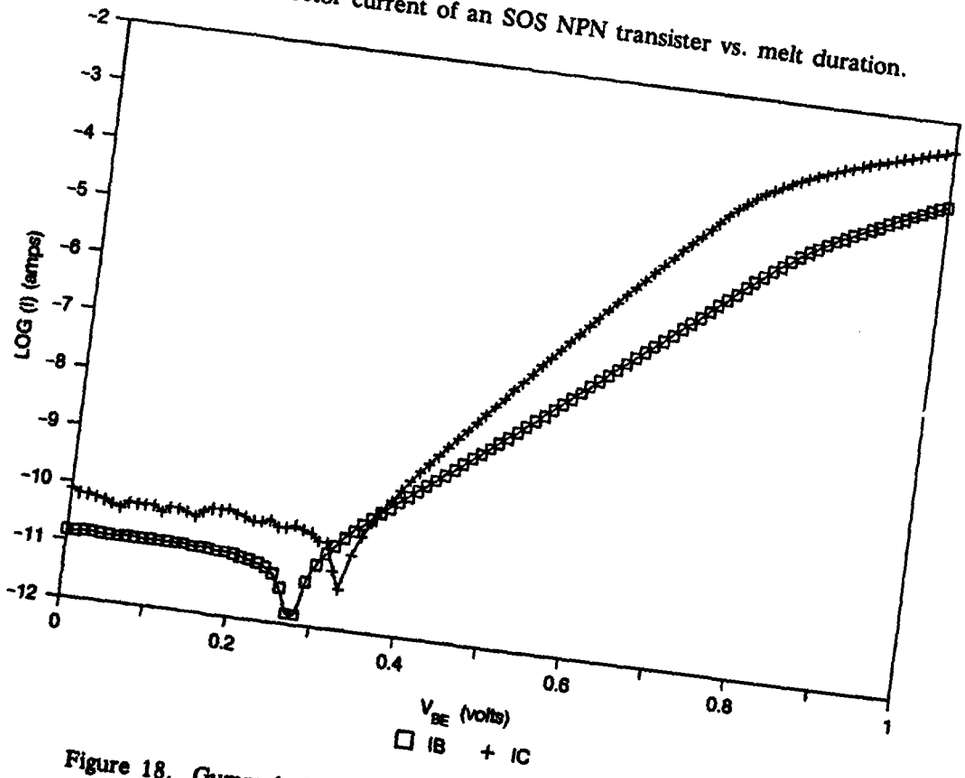


Figure 18. Gummel plot of bulk wafer 3, 83 ns, 1x8 μm emitter.

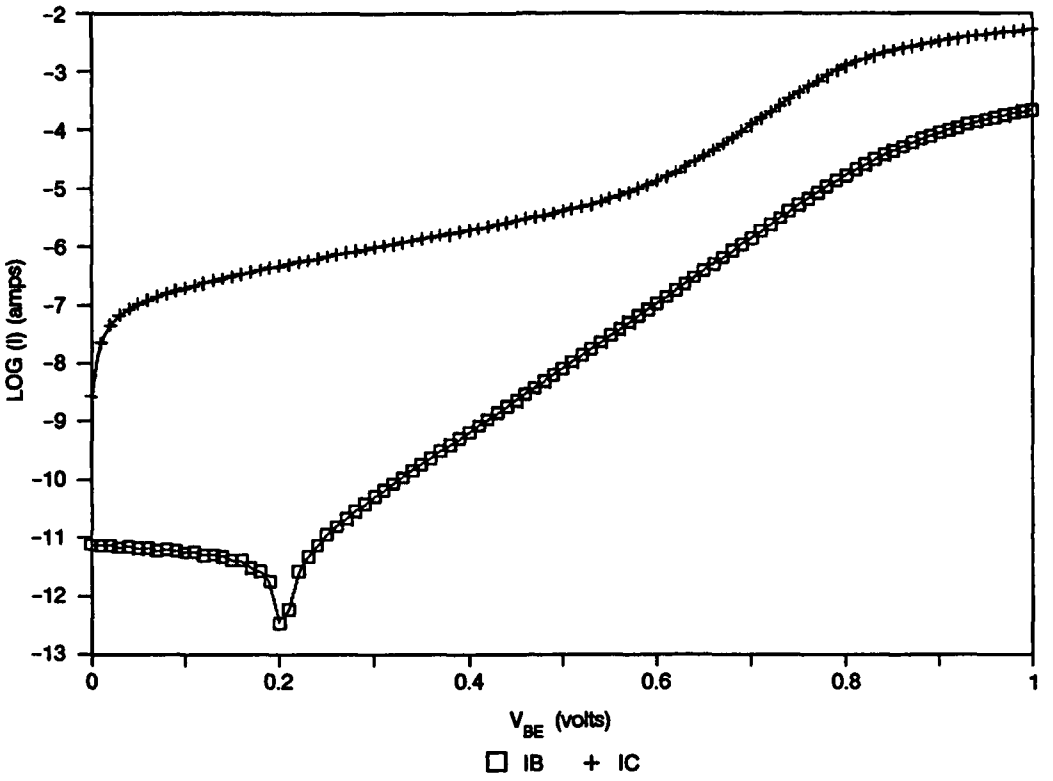


Figure 19. Gummel plot of wafer D70, 83 ns, 1x8 μm emitter.

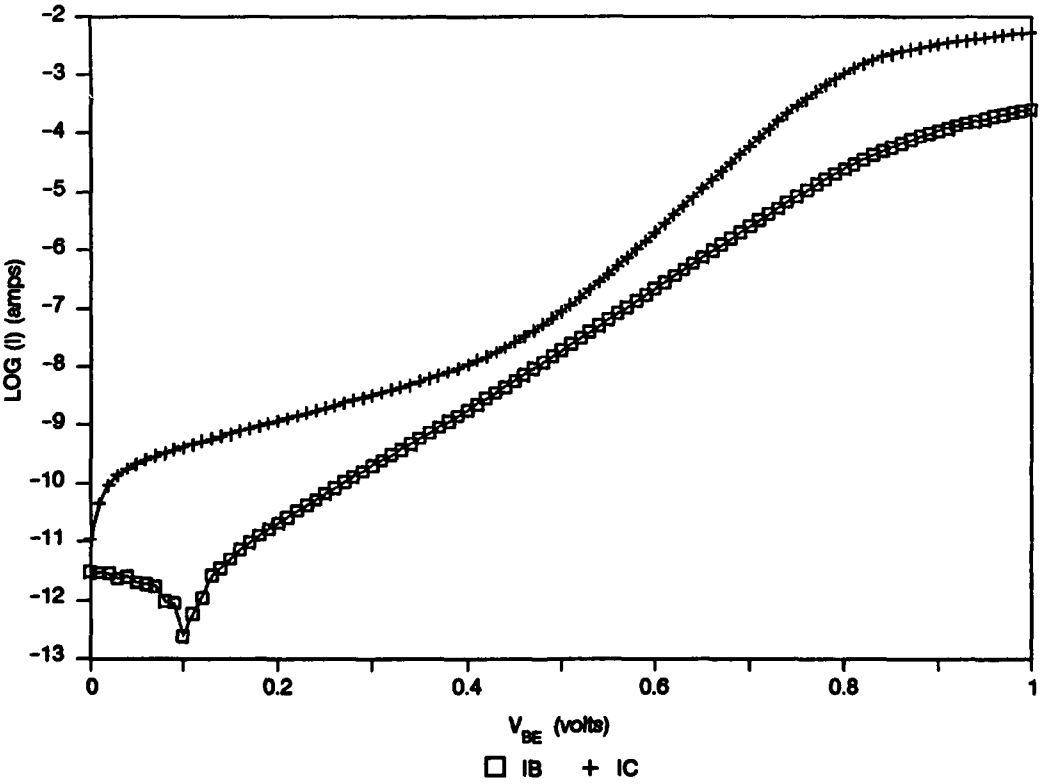


Figure 20. Gummel plot of wafer D70, 68 ns, 1x8 μm emitter.

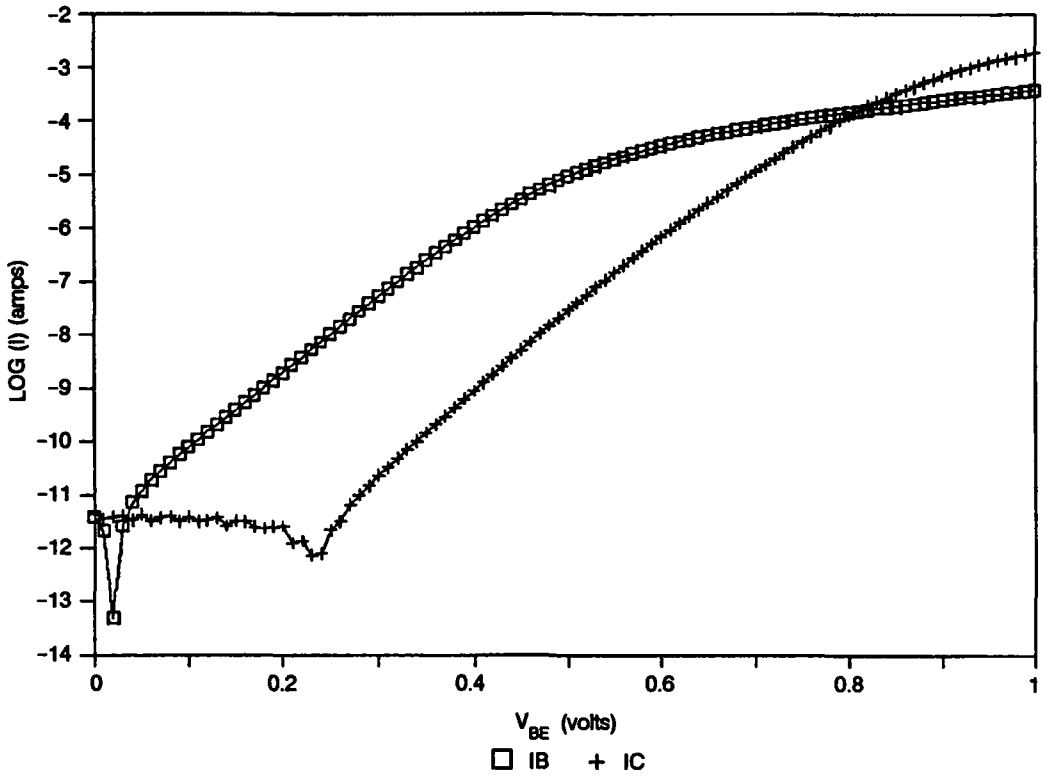


Figure 21. Gummel plot of wafer D70, 57 ns, 1x8 μm emitter.

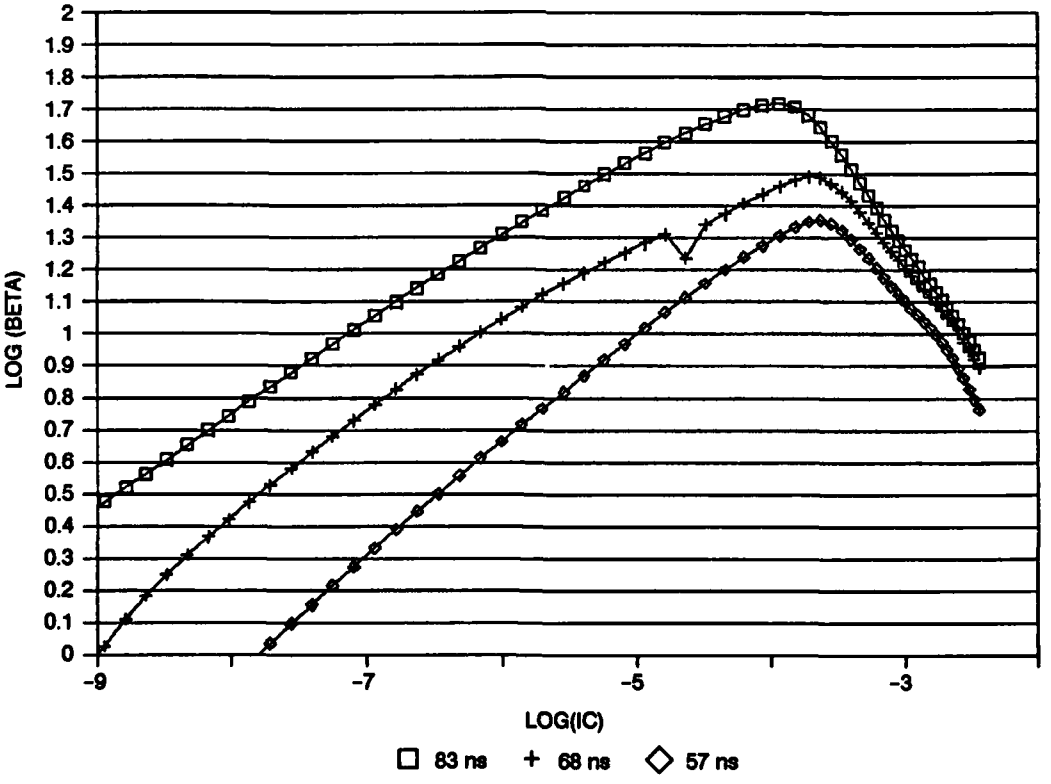


Figure 22. Beta vs. IC, wafer 3.

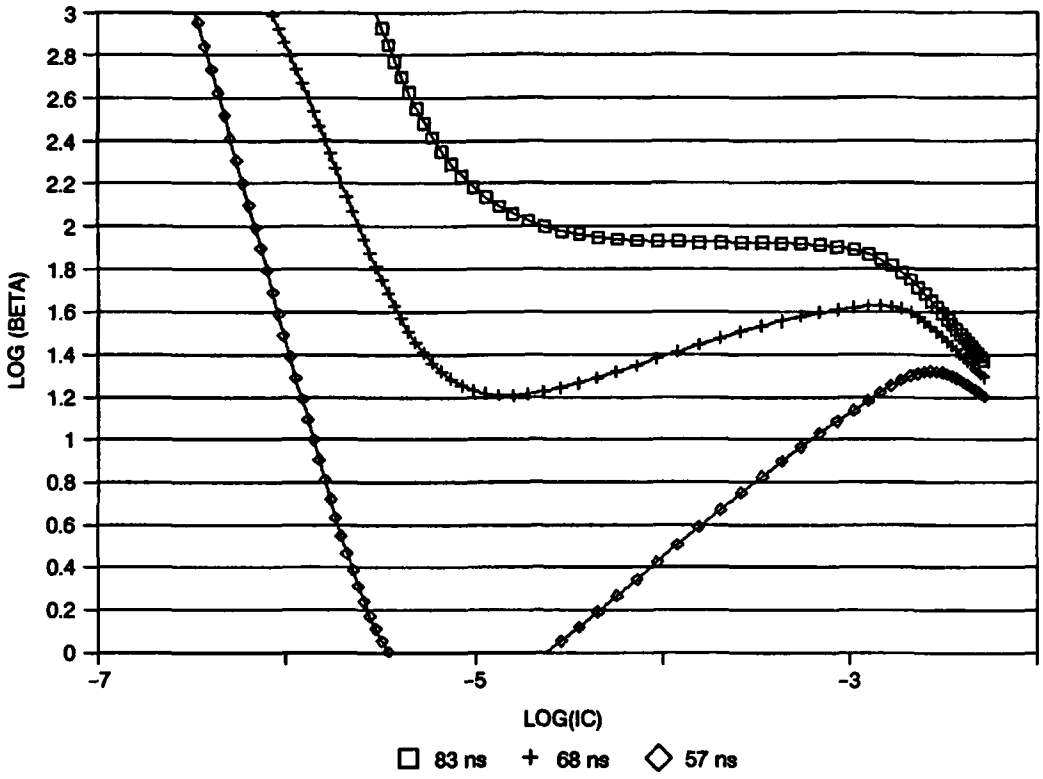


Figure 23. Beta vs. IC, wafer D70.

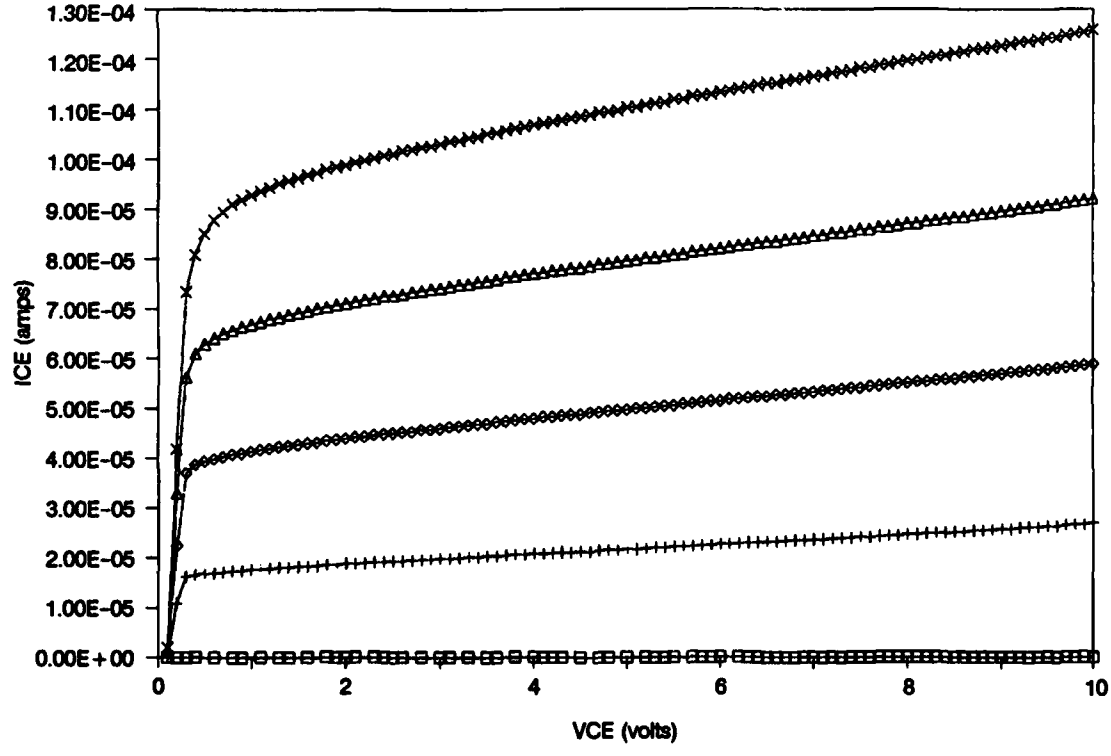


Figure 24. IC vs. VCE family of curves for bulk wafer 3, 83-ns emitter, 500-nA steps.

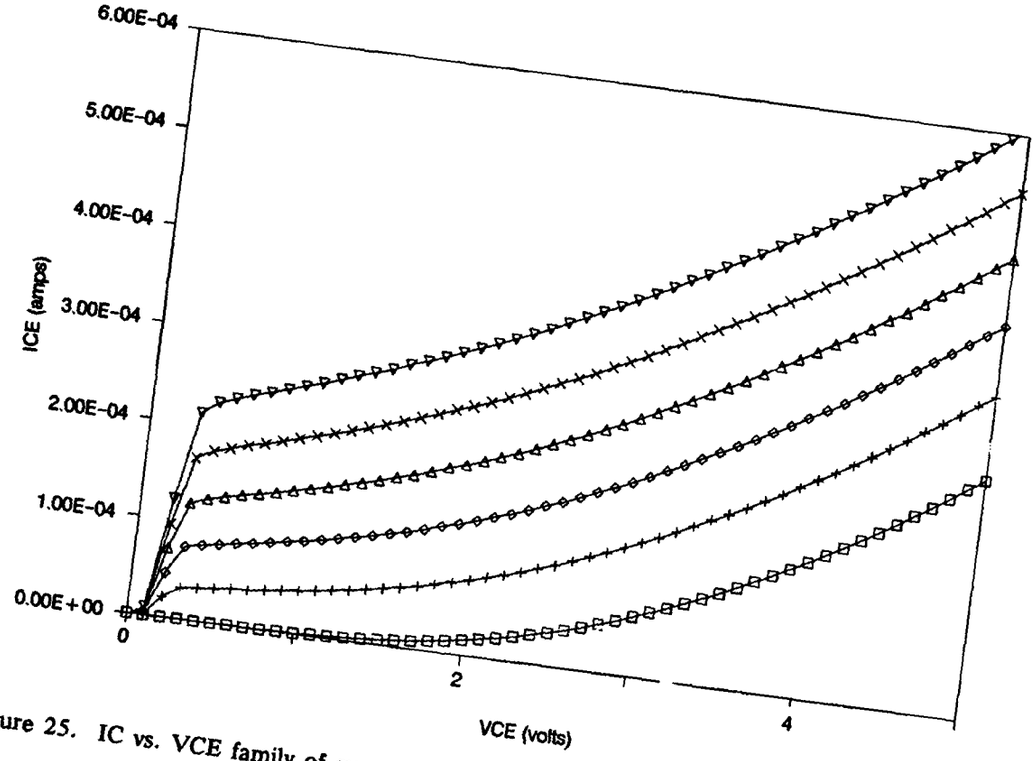


Figure 25. IC vs. VCE family of curves for SOS wafer D71, 83-ns emitter, 500-nA steps.

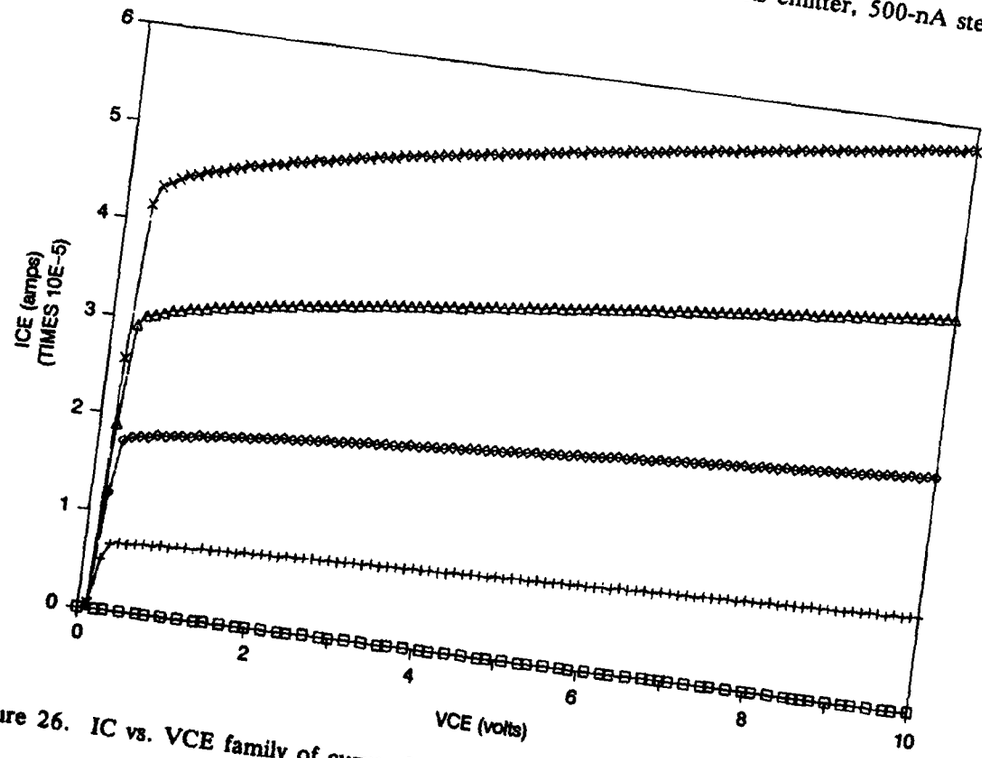


Figure 26. IC vs. VCE family of curves for bulk wafer 3, 57-ns emitter, 500-nA steps.

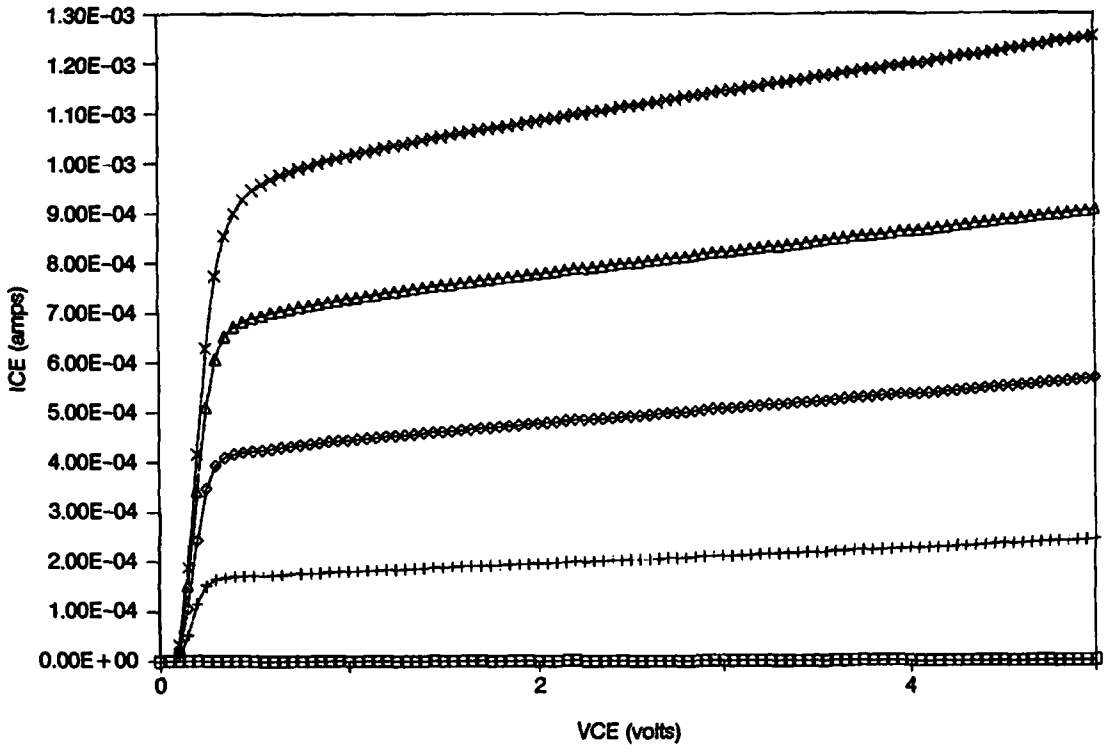


Figure 27. IC vs. VCE family of curves for SOS wafer D71, 57-ns emitter, 10-μA steps.

CONCLUSION

Bipolar transistors on bulk silicon and SOS material were fabricated by using laser processing in an attempt to mitigate the deleterious effects on device behavior of the poor crystalline quality of SOS material. Base widths of 500 to 1500 Å and corresponding gains of 94 to 12 were achieved on SOS material. Non-ideal behavior has been attributed to defects and unannealed implant damage. Laser processing seems to have improved leakage on the SOS by not allowing dopant to diffuse through junctions by means of diffusion pipes. This improvement was due to the rapid recrystallization (less than 100 ns) of the silicon material. Continued research into and the development of epitaxial SOS growth techniques at NOSC and improvements of the laser process suggested in this paper may lead to device performance comparable to or exceeding that of bulk silicon devices.

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B. W. Offord, S. D. Russell, K. H. Weiner

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Nanosecond thermal processing using an excimer laser was used in the fabrication of NPN bipolar transistors in silicon-on-sapphire (SOS). Functional devices with current gain approaching 100 were obtained. The deleterious effects of diffusion pipes in SOS material were minimized using rapid laser activation of ion implanted dopant. Details of the device design, fabrication, and test results are included in this report.

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